AMENDMENTS TO THE CLAIMS

1. (cancelled)

2. (currently amended) The method of claim ~~1~~4, further comprising forming a silicide layer on said upper polysilicon region.

3. (currently amended) The method of claim ~~1~~4, wherein said conductive barrier is selected from the group of: tungsten nitride (WN), tantalum nitride (TaN), titanium nitride (TiN), tungsten silicon nitride (WSiN), tantalum silicon nitride (TaSiN), aluminum titanium nitride (AlTiN), titanium silicide (TiSi),quantum conductive semi-insulating barriers, and combinations comprising at least one of the foregoing.

4. (currently amended) ~~The method of claim 1,~~ A method for forming a gate structure for a semiconductor transistor, the method comprising:

forming a lower polysilicon region on a gate dielectric layer;

implanting said lower polysilicon region with a dopant at a first dopant concentration;

forming a conductive barrier layer upon said lower polysilicon region;

forming an upper polysilicon region upon said conductive barrier layer; and

implanting said upper polysilicon region with dopant at a second dopant concentration, said second concentration being different than said first concentration;

wherein said lower polysilicon region comprises silicon germanium carbon (SiGeC).

5. (currently amended) ~~The method of claim 1,~~ A method for forming a gate structure for a semiconductor transistor, the method comprising:

forming a lower polysilicon region on a gate dielectric layer;

implanting said lower polysilicon region with a dopant at a first dopant concentration;

forming a conductive barrier layer upon said lower polysilicon region;

forming an upper polysilicon region upon said conductive barrier layer; and

implanting said upper polysilicon region with dopant at a second dopant concentration, said second concentration being different than said first concentration;

wherein said lower polysilicon region is doped at a concentration of about 1×10^{21} atoms/cm^3, and said upper polysilicon region is doped at a concentration of about 3×10^{20} atoms/cm^3.

6. (currently amended) ~~The method of claim 1, wherein said lower polysilicon region is formed by:~~ A method for forming a gate structure for a semiconductor transistor, the method comprising:

forming a lower polysilicon region on a gate dielectric layer by defining a polysilicon block on said gate dielectric layer~~;~~, forming a sacrificial layer over said gate dielectric layer and said polysilicon block~~;~~, planarizing said sacrificial layer down to the top of said polysilicon block~~,~~; and recessing said polysilicon block below the top of the planarized sacrificial layer;

implanting said lower polysilicon region with a dopant at a first dopant concentration;

forming a conductive barrier layer upon said lower polysilicon region;

forming an upper polysilicon region upon said conductive barrier layer; and

implanting said upper polysilicon region with dopant at a second dopant concentration, said second concentration being different than said first concentration.

7. (currently amended) The method of claim ~~1~~4, wherein said upper polysilicon region is formed directly upon a top surface of said conductive barrier layer.

8. (currently amended) The method of claim ~~14~~, wherein said second concentration is less than said first concentration.

9. (new) The method of claim 5, further comprising forming a silicide layer on said upper polysilicon region.

10. (new) The method of claim 5, wherein said conductive barrier is selected from the group of: tungsten nitride (WN), tantalum nitride (TaN), titanium nitride (TiN), tungsten silicon nitride (WSiN), tantalum silicon nitride (TaSiN), aluminum titanium nitride (AlTiN), titanium silicide (TiSi),quantum conductive semi-insulating barriers, and combinations comprising at least one of the foregoing.

11. (new) The method of claim 5, wherein said upper polysilicon region is formed directly upon a top surface of said conductive barrier layer.

12. (new) The method of claim 6, further comprising forming a silicide layer on said upper polysilicon region.

13. (new) The method of claim 6, wherein said conductive barrier is selected from the group of: tungsten nitride (WN), tantalum nitride (TaN), titanium nitride (TiN), tungsten silicon nitride (WSiN), tantalum silicon nitride (TaSiN), aluminum titanium nitride (AlTiN), titanium silicide (TiSi),quantum conductive semi-insulating barriers, and combinations comprising at least one of the foregoing.

14. (new) The method of claim 6, wherein said upper polysilicon region is formed directly upon a top surface of said conductive barrier layer.

15. (new) The method of claim 6, wherein said second concentration is less than

said first concentration.